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Research Article

Design of Scan Chain Based Fault Tolerant Parallel Filters to Recover Multiple Errors

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Abstract: In our today's world the communication without the fault can be required. In signal processing there are many filters can be achieved for the communications such as the digital filters, FIR filters and the parallel filters. For the kind of error fault detection the parallel filters must be suited for the high level applications. The parallel filters with fault tolerance have been proposed here to detect the multiple errors present in the communication channels. The error recovery could be done by using the hamming code and the extended hamming codes. The hamming code can be proposed for the single bit error tolerance and the extended hamming code can be achieved for the multiple bit error detection. The fault tolerance architecture having this error correction method can be very less power, area and the delay consumption. The parallel filter architecture with error correction must be suitable for the high stable communication with high reliability. The most required system for the applications may be considered for the single event test in the parallel architecture. The high secure communication with the multiple bit errors can also to be recognized from the channel length of the input signal. This architecture can be less latency with its high number of the latches. The on-data path pipelines for this process can be varied from the structure for the event based signals. These hamming codes with the error detection and correction for the single bit and the multiple bits can be achieved. The process variation and its implementation can be achieved by using the Xilinx ISE software. The power analysis can be done through the X power analyzer.
Keywords: Hamming code, multiple error, Error correction and detection.

INTRODUCTION

On-chip packet-switched communication [1] is projected as an answer for the matter of world interconnects in deep submicron VLSI Error Correction codes (ECC). Error Correction codes (ECC) will [6] address and contain major physical problems such as synchronization, noise, error-correction and speed optimization. Secret agent [5] will conjointly improve style productivity by supporting [2] modularity and utilize of advanced cores, so enabling the next level of abstraction in beaux arts modelling of future systems [4]. However, VLSI designers should be ensured that the advantages of secret agent don't compromise system performance and price [8].

Performance issues square measure associated with latency and turnout. Value issues square measure primarily chip-area and power dissipation [12]. This paper presents a error correction method and a network architecture design that satisfy hamming encoding requirements at a measurable VLSI value that is favourably [8] compared with various error detection interconnection approaches. Traditionally, this world communication has been [10] self-addressed by shared-bus structures and ad-hoc direct interconnections. Non-scalability of those approaches was mentioned in [9]. However, fashionable error correction buses have evolved to multi-layered and mesmeric structures, supporting [4] split transactions, burst transfers and parallel operations [4].

From many aspects they can be thought-about as networks however still, they don't offer effective abstraction utilize of resources and [7] do not utilize packet or wormhole change related to distributed routing and congestion/flow management. Therefore, they're inefficient and need centralized [8] arbitration mechanisms. Advantages of spatial-reuse packet/wormhole switched networks were analysed compared with buses by many authors [9]. A hybrid approach, supporting each secret agent and on-chip buses has been projected in [10].

The hamming encoding method and techniques for his or her style are developed for pc networks and for digital computer systems [1]. However, a unique set of resource constraints and style concerns exists for associate degree single and the multiple error setting. As represented in [9], memory and computing resources square measure comparatively costlier on-chip, whereas comparatively [11] a lot of wires square measure accessible. The necessity to mix several styles of service, like "best effort" and "guaranteed throughput" was noted by [8]. In [9] it absolutely was prompt to support several access paradigms like request-response (for compatibility with bus-based approaches) and connection-oriented services for extended practicality. A mesh constellation was projected in [4] a torus topology was projected in [1], whereas [6] used a fat tree. Completely different routing schemes and router architectures are projected. G

Unlike laptop networks that area unit designed for on-going growth, future growth and standards compatibility, digital filters and its requirement can be designed and customized for a-priori best-known [9] set of computing resources, given pre-characterized traffic patterns among them. These imply that varied elements of the specification together with addressing [5] fields and communication filters such as parallel filters classification will be modified between implementations. The physical layer is optimized to require care of deep-submicron problems like delay [4] and repeater improvement, synchronization, noise immunity etc. The error recovery applies a mesh topology and employs hollow packet forwarding with hop-by-hop credit-based backpressure flow control [5].

The method for the correction and the detection of the errors [5] in the single or multiple input channels through communication must be better [2] for its architecture. The developing communication must be either can be developed from the architectures which [6] will be used as the hamming encoding techniques. The other implementation process also be [9] recognized and then achieved by using this proposed method [11].

PARALLEL FILTERS AND ERROR CORRECTION CODES

The parallel filters are the filters that can be used in the filter bank for the communication channel in the protection status. The data's communicated through this channel lenght have been arrived from the associated architecture. The parallel filter equation as been shown below:

$$y[n] = \sum_{l=0}^{\infty} x[n-l] \cdot h[l]$$

where y[n] is the output signal x[n] is the input signal and the impulse responses has been arranged as h[l]. The impulsive responses from the rate of all the sections in the whole architecture have been analyzed. The shown figure has been analyzed from the various input and the output signals.

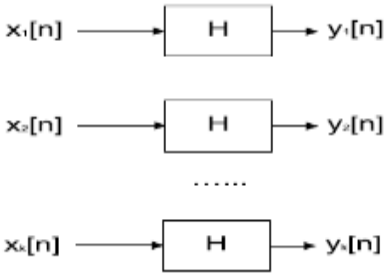

Fig-1: Parallel filter implementation with some responses

The error correction codes can be easily enabled with the input and the output signals for the hamming code architecture. This will be recovered from the each input sizes of the data's from the input of x[n]. The values can be varied for the each and every input data's such as high and the low level channel lengths. Error correction codes (ECC) has been delivered as the throughput of the process variation from the internal structure of the architecture. These signal also to be varied in front of the data transmission lines and the recovered signals. At last where the fault is occur through the whole data signal using the channel length. The fault tolerance filter has been achieved from the structure that could be arrived in front of the realized data unit. The multiple data error has been detected from the input data using the hamming code. The single bit error has been detected and then it will be corrected over the all channel length. This will be followed from the whole process to detect and correct the errors.

HAMMING CODES

Hamming codes are the protection codes which will be used in all the communication networks where security need be more. These codes are error detecting and correction codes for the process of the data transmit and receive. The original bits are added with the redundant bits to reduce the security and losses of the information. This will be highly rescued using the hamming codes.

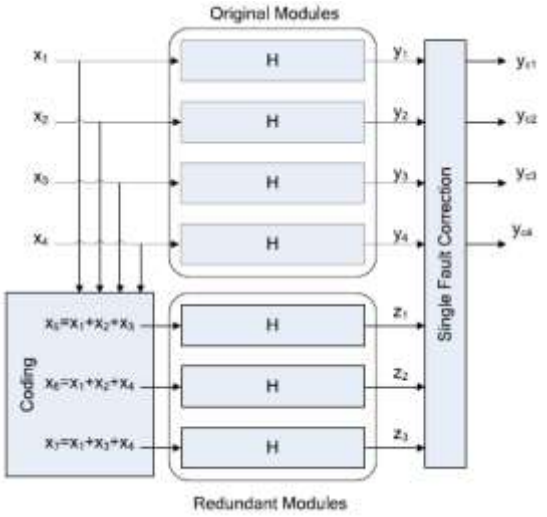

Fig-2: Architecture for the hamming code

In this method the input parity bits are to be added as x1, x2, x3, x4... with these entries. The data bit error can be added in the original modules for the recovered data entries. The valuable bits can be corrected as per the request present in the input data. The redundant module bits can also to be added in the original modules. The output data bits could be received from the module which can be corrected with the fault. The error detection can be done through this section which will be carried out for the data bit loading section. The fault tolerant modules which could show in the hamming code architecture. The output fault tolerant bits to be achieved as y_{c1}, y_{c2}, y_{c3}, y_{c4}. The computing method from the achieved bit error rate can be considered as the powered bits as parity checker. The reliable functions which could be having the input error bits as p1, p2, p3 and also the action required bits could be as d1, d2, d3. The receive signals from the structure oriented error rate for the faults that could be present in the considered signals.

Then the module values are as follows:

- x_3, x_5, x_6, x_7 are chosen according to the message (perhaps the message itself is (x_3 x_5 x_6 x_7)).
- $x_4 := x_5 + x_6 + x_7 \pmod 2$
- $x_2 := x_3 + x_6 + x_7$
- $x_1 := x_3 + x_5 + x_7$

The modules with the fault tolerant can be added in the error rate for the output modules in the signals to be as d1, d2, d3, d4. These error actions taken bits are also to be considered for the original modules which would be having these same $y = x \bullet G$ for the computing module. The parity check bits for those filters as it are shown for the x and H level structures. These are to be calculated from the bits with the error with the fault correction and the detection. This could be suited for the single bit error rate for fault tolerant.

Filters rate and the parallel filter check bits could be,

$$z_1[n] = \sum_{l=0}^{\infty} \left(x_1[n-l] + x_2[n-l] + x_3[n-l]\right) \cdot h[l]$$

$$z_2[n] = \sum_{l=0}^{\infty} \left(x_1[n-l] + x_2[n-l] + x_4[n-l]\right) \cdot h[l]$$

$$z_3[n] = \sum_{l=0}^{\infty} \left(x_1[n-l] + x_3[n-l] + x_4[n-l]\right) \cdot h[l]$$

And then the testing filter values could be as,

$$z_1[n] = y_1[n] + y_2[n] + y_3[n]$$
$$z_2[n] = y_1[n] + y_2[n] + y_4[n]$$
$$z_3[n] = y_1[n] + y_3[n] + y_4[n].$$

The final filtering equation could be shown and also the error rate can be calculated as much as from the required data bit to the relevant inputs. The generating values as G and the original module bits as H for the required bits can be added in the redundant data's. The final structure with this error rate and the final fault could be measured over the signals by using the above equations. The y[n] and z[n] values could be considered for the single bit error detection and the correction method.

MODIFICATION

In the proposed method we are going to implement the extended hamming code for the multiple bit errors with error detection. The parity bits are to be taken as the input original modules with the redundant bits such as x5, x6, x7, and x8. With this extended code we are going to add the multiple bit errors with the parity bits through the original modules for the fault detection. Hamming code rules are to be added in the bits transition for the making of hamming encoding algorithm.

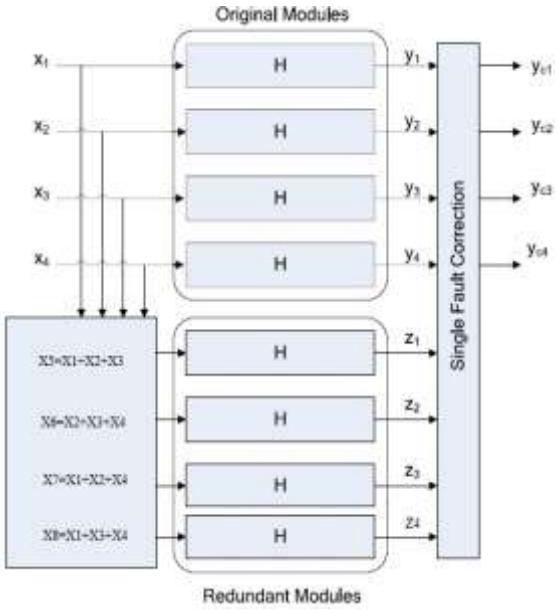

Fig-3: Architecture for the extended hamming code

The distance between the code word has to be taken and the results to be analyzed as per the input parity bits. The related code word method to be achieved as per the message bits such as the x0 to x7. The parity check bits with the reliable communication for error detecting has been checked for this identification to the x[n] into the y[n] values.

x1, x2, x3, x4 are chosen according to the message.

- x5 = x1 + x2 + x3
- x6 = x1 + x2 + x4
- x7 = x1 + x3 + x4

Add a new bit x_0 such that

- $x_0 = x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7$. i.e., the new bit makes the sum of all the bits zero. x_0 is called a parity check**.**

The binary hamming code construction method to be analyzed as per the distance for [2r, 2r-1 - r] extended code from a [2r –1, 2r –1 – r] to the various bits. The area and the delay consumption to be calculated as per the distance from the code word resources. The power can also to be added as per the detailed information for the gate level implementation to the parallel filters. The fault recognition could be added in this architecture for the error action bits such as d1, d2, d3, d4. These are also called to be as multiple bit error detection and correction codes.

The parity check matrix also is added in the original bit data for the most reliable communication in the sector. The parity checking matrix G and H are as follows:

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}.$$

Then finally the error location can be found and then the action can be taken from the structure which is to be needed for the error detection in the extended hamming code. The output for these parity bits can be y1, y2, y3, y4 and z1, z2, z3, z4. This can be for the parallel filter architecture without the fault detection. When the multiple bit fault detection can be added in the signals then the output function could be more and more effective with channel length such as y_{c1}, y_{c2}, y_{c3}, y_{c4}. The most suitable bit function with the fault can be detected for the multiple bits with the error bits as the original data. The consideration for the error correction in the signal level transition cannot be made for the error detection in these bits.

SIMULATION RESULTS

The hamming code architecture simulation can be done through the Xilinx ISE using HDL. The data address bit verification can also to be done through this simulation and the waveform could be verified by using the MODELSIM. And also we analyzed the area delay analysis in this process. The power analysis for this architecture can be done through the X power analyzer. The results could be simulated and then shown in the below diagram.

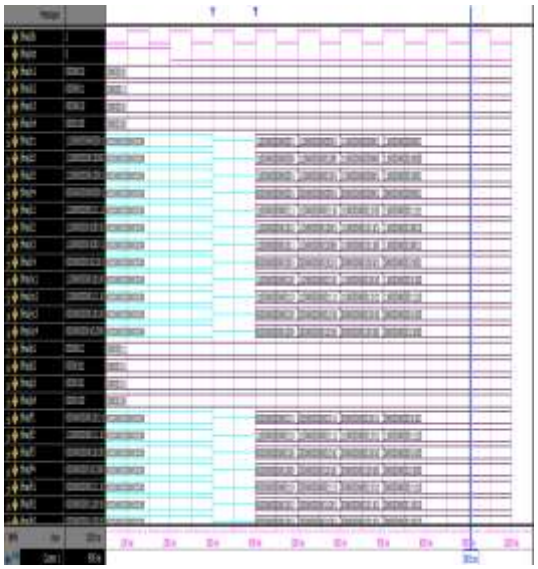

Fig-4: Waveform for the hamming code error correction

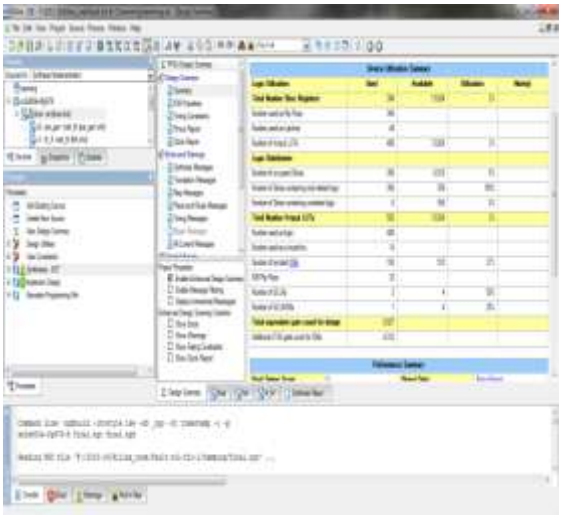

Fig-5: Diagram of Area analysis of the hamming code

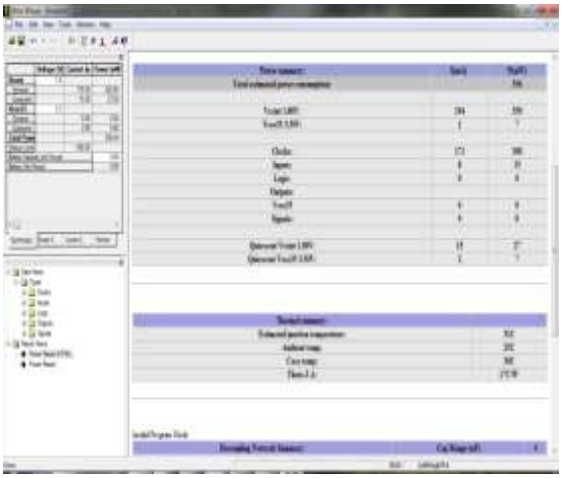

Fig-6: Power analysis of the hamming code

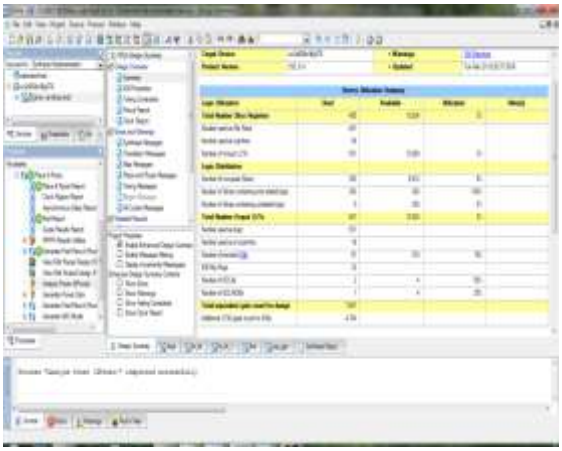

Fig-7: Area analysis of the extended hamming code

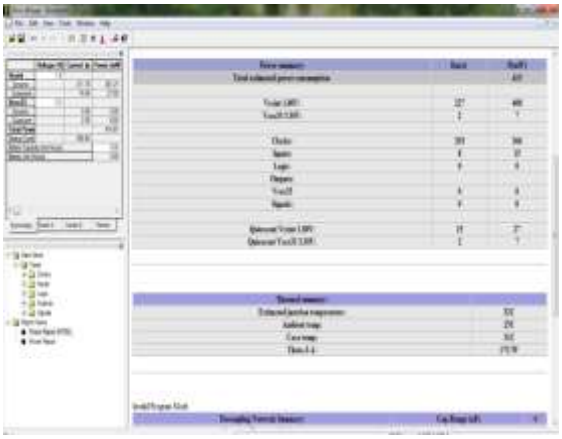

Fig-8: Power analysis of the extended hamming code

CONCLUSION

In this paper we have proposed the extended hamming code for the parallel filters including the multiple bits. The data error correction and the detection can also to be done through this system architecture for the calculation of the area, delay and the power consumption values. The resulted architecture data's for the extended hamming algorithm to be considered for the error action should be taken. The architecture can be suited for the high secure communication with the data transfer over the high channel length. The computation process can to be analyzed for the existing and proposed hamming code architecture. The multiple bits and the single bit error have been detected over the channel for parallel filters. The fault tolerance over the channel decade can be used for the parallel filters with its hardware implementation also.

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